

In the claims

1. (Currently Amended) A low drop-out voltage regulator comprising:
transistor means for receiving a reference voltage and in dependence thereon producing a regulated output voltage [[:]], the transistor means having an output stage for coupling to a load; and
~~first direct current (DC) control loop means coupled to the transistor means for providing a dominant pole; and wherein~~
~~second direct current (DC) control~~ the transistor means further comprises at least part of output loop means, the output loop means for providing a non-dominant pole, whereby low output impedance for coupling across the load so as to provide stability of operation may be obtained with a lower by lowering a load-capacitance of the load.
2. (Original) The low drop-out voltage regulator as claimed in claim 1 wherein the control loop means comprises:
differential amplifier means having an output coupled to the transistor means; and
voltage divider means coupled between the voltage regulator output and a first input of the differential amplifier means.
3. (Original) The low drop-out voltage regulator as claimed in claim 2 wherein the control loop means further comprises:
voltage reference means coupled between the voltage regulator output and a first input of the differential amplifier means.
4. (Previously presented) The low drop-out voltage regulator as claimed in claim 1 wherein the output stage comprises a low impedance output.
5. (Currently amended) A The low drop-out voltage regulator as claimed in claim 1 wherein the ~~second direct current (DC) control~~ output loop means is coupled to the voltage regulator output and ~~first direct current (DC) the~~ control loop means.

6. (currently amended) A ~~The~~ low drop-out voltage regulator as claimed in claim 1 wherein the ~~second direct current (DC)-control~~ output loop means has a unity direct current (DC) gain.
7. (Previously presented) The low drop-out voltage regulator as claimed in claim 1 wherein the transistor means comprises a cascode transistor arrangement.
8. (Previously presented) The low drop-out voltage regulator as claimed in claim 1 wherein the output stage comprises a cascode transistor arrangement.
9. (Previously presented) The low drop-out voltage regulator as claimed in claim 1 wherein the output stage comprises a P-type transistor.
10. (Original) The low drop-out voltage regulator as claimed in claim 9 wherein the P-type transistor is a PMOS transistor.
11. (Cancelled)
12. (Currently Amended) A method for low drop-out voltage regulation comprising:
 - providing transistor means receiving a reference voltage and in dependence thereon producing a regulated output voltage; the transistor means having providing an output stage for coupled coupling to a load; and
 - providing ~~first direct current (DC)-control~~ loop means coupled to the transistor means for providing a dominant pole; and wherein
 - second direct current (DC)-control the transistor means further comprises at least part of output loop means, the output loop means and-providing a non-dominant pole, whereby low output impedance for coupling across the load so as to provide stability of operation may be obtained with a lower by lowering a load capacitance of the load.
13. (Original) The method for low drop-out voltage regulation as claimed in claim 12 wherein the control loop means comprises:
 - differential amplifier means having an output coupled to the transistor means; and
 - voltage divider means coupled between the voltage regulator output and a first input of the differential amplifier means.

14. (Original) The method for low drop-out voltage regulation as claimed in claim 13 wherein the control loop means further comprises:

voltage reference means coupled between the voltage regulator output and a first input of the differential amplifier means.

15. (Previously presented) The method for low drop-out voltage regulation as claimed in claim 12 wherein the output stage comprises a low impedance output.

16. (Currently amended) The method for low drop-out voltage regulation as claimed in claim 12 wherein the ~~second direct current (DC) control output~~ loop means is coupled to the voltage regulator output and ~~first direct current (DC) the~~ the control loop means.

17. (Currently amended) The method for low drop-out voltage regulation as claimed in claim 12 wherein the ~~second direct current (DC) control output~~ loop means has a unity direct current (DC) gain.

18. (Previously presented) The method for low drop-out voltage regulation as claimed in claim 12 wherein the transistor means comprises a cascode transistor arrangement.

19. (Previously presented) The method for low drop-out voltage regulation as claimed in claim 12 wherein the output stage comprises a cascode transistor arrangement.

20. (Previously presented) The method for low drop-out voltage regulation as claimed in claim 12 wherein the output stage comprises a P-type transistor.

21. (Currently Amended) The method for low drop-out voltage regulation as +claimed in claim 20 wherein the P-type transistor is a PMOS transistor.

22. (Cancelled)

23. (Previously amended) An integrated circuit comprising the low drop-out voltage regulator of claim 1.